

8-28-03

Form PTO-1449 (Modified)		Atty Docket No.: 42P17280		Serial No.: <del>Unknown</del> 10/652796	
List of Patents and Publications Statement (Use several sheets if necessary)				Applicant: Justin K. Brask et al.	
				Filing Date: Herewith 8-28-03	

REFERENCE DESIGNATION			U.S. PATENT DOCUMENTS			
Examiner Initials		Document No.		Class	Sub-Class	Filing date if appropriate
<i>JMB</i>	AA	5,625,217	Chau et al.	257	412	
<i>JMB</i>	AB	5,753,560	Hong et al.	438	402	
<i>JMB</i>	AC	5,783,478	Chau et al.	438	592	
<i>JMB</i>	AD	5,891,798	Doyle et al.	438	624	
<i>JMB</i>	AE	6,063,698	Tseng et al.	438	585	
<i>JMB</i>	AF	6,087,261	Nishikawa et al.	438	685	
<i>JMB</i>	AG	6,184,072	Kaushik et al.	438	197	
<i>JMB</i>	AF	6,306,742 B1	Doyle et al.	438	591	
<i>JMB</i>	AI	6,391,802 B1	Delpech et al.	438	785	
<i>JMB</i>	AJ	6,420,279	Ono et al.	48	785	
<i>JMB</i>	AK	6,475,874	Xiang et al.	438	396	
<i>JMB</i>	AL	6,544,906	Rotondaro et al.	438	785	
<i>JMB</i>	AM	US2003/032303	Yu et al.	438	770	

FOREIGN PATENT DOCUMENTS							
		Document No.	Date	Country	Class	Sub-Class	Translation
	AM						
	AN						

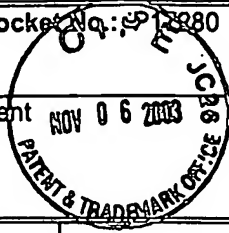
OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
<i>JMB</i>	AO	Doug Barlage et al., "High-Frequency Response of 100nm Integrated CMOS Transistors with High-K Gate Dielectrics", 2001 IEEE, 4 pages.
<i>JMB</i>	AP	Robert Chau et al., "A 50nm Depleted-Substrate CMOS Transistor (DST), 2001 IEEE, 4 pages.
<i>JMB</i>	AQ	Lu et al., "Dual-Metal Gate Technology for Deep-Submicron CMOS Devices", dated April 29, 2003, 1 page.
<i>JMB</i>	AR	Schwantes et al., "Performance Improvement of Metal Gate CMOS Technologies with Gigabit Feature Sizes", Technical University of Hamburg-Harburg, 5 pages.
<i>JMB</i>	AS	Chau et al., "A Method of Making Semiconductor Device Having a High-K Gate Dielectric", Serial No. 10/082,530, Filed February 22, 2002
<i>JMB</i>	AT	Parker et al., "A Method of Making Semiconductor Device Having a High-K Gate Dielectric", Serial No. 10/285,915, Filed October 31, 2002
<i>JMB</i>	AU	Chau et al., "A Method of Making Semiconductor Device Having a High-K Gate Dielectric", Serial No. 10/288,043, Filed November 5, 2002
<i>JMB</i>	AV	Parker et al., "A Method of Making Semiconductor Device Having a High-K Gate Dielectric", Serial No. 10/315,268, Filed December 10, 2002
<i>JMB</i>	AW	Doczy et al., "A Method of Making Semiconductor Device Having a High-K Gate Dielectric", Serial No. 10/338,174, Filed January 7, 2003
<i>JMB</i>	AX	Brask et al., "A Method of Making Semiconductor Device Having a High-K Gate Dielectric", Serial No. 10/387,303, Filed March 11, 2003
<i>JMB</i>	AY	Brask et al., "A Method of Making Semiconductor Device Having a High-K Gate Dielectric", Serial No. 10/391,816, Filed March 18, 2003
<i>JMB</i>	AZ	Chau et al., "A Method for Making a Semiconductor Device Having a Metal Gate Electrode", Serial No. 10/431,166, Filed May 6, 2003
<i>JMB</i>	BA	Brask, et al., "A Method for Making a Semiconductor Device Having a High-K Gate Dielectric", Serial No. 10/441,616, filed May 20, 2003

Examiner <i>George M. Mc</i>	Date Considered 2/3/05
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11-6-03

Form PTO-1449 (Modified)		Atty Docket No.: 912880		Serial No.: 10/652,796	
List of Patents and Publications Statement (Use several sheets if necessary)				Applicant: Justin K. Brask et al.	
				Filing Date: August 28, 2003	



REFERENCE DESIGNATION			U.S. PATENT DOCUMENTS			
Examiner Initials		Document No.		Class	Sub-Class	Filing date if appropriate
<i>JMB</i>	AA	6,121,094	Gardner et al.	438	287	
<i>JMB</i>	AB	6,436,777	Ota	438	305	
<i>JMB</i>	AC	6,514,828	Ahn et al.	438	297	
<i>JMB</i>	AD	6,617,209	Chau et al.	438	240	
<i>JMB</i>	AE	6,617,210	Chau et al.	438	240	
<i>JMB</i>	AF	US2002/0197790	Kizilyalli et al.	438	240	
<i>JMB</i>	AG	US2003/0045080	Visokay et al.	438	591	
	AH					
	AI					
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FOREIGN PATENT DOCUMENTS							
No.		Document No.	Date	Country	Class	Sub-Class	Translation
	AQ						
	AR						
	AS						
	AT						
	AU						

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
<i>JMB</i>	AV	Polishchuk et al., "Dual Workfunction CMOS Gate Technology Based on Metal Interdiffusion," <a href="http://www.eesc.berkeley.edu">www.eesc.berkeley.edu</a> , 1 page.
	AW	
	AX	
	AY	
	AZ	

Examiner <i>Shirley M. Mc</i>	Date Considered <i>2/3/05</i>
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.